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| Tool Version : Vivado v.2014.4 (win64) Build 1071353 Tue Nov 18 18:24:04 MST 2014

| Date : Mon Apr 06 14:08:06 2015

| Host : George-PC running 64-bit Service Pack 1 (build 7601)

| Command : report\_utilization -file top\_utilization\_synth.rpt -pb top\_utilization\_synth.pb

| Design : top

| Device : xc7a35t

| Design State : Synthesized

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Utilization Design Information

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1. Slice Logic

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| Site Type | Used | Fixed | Available | Util% |

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| Slice LUTs\* | 166 | 0 | 20800 | 0.79 |

| LUT as Logic | 166 | 0 | 20800 | 0.79 |

| LUT as Memory | 0 | 0 | 9600 | 0.00 |

| Slice Registers | 98 | 0 | 41600 | 0.23 |

| Register as Flip Flop | 98 | 0 | 41600 | 0.23 |

| Register as Latch | 0 | 0 | 41600 | 0.00 |

| F7 Muxes | 0 | 0 | 16300 | 0.00 |

| F8 Muxes | 0 | 0 | 8150 | 0.00 |

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\* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt\_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

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| Total | Clock Enable | Synchronous | Asynchronous |

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| 0 | \_ | - | - |

| 0 | \_ | - | Set |

| 0 | \_ | - | Reset |

| 0 | \_ | Set | - |

| 0 | \_ | Reset | - |

| 0 | Yes | - | - |

| 0 | Yes | - | Set |

| 0 | Yes | - | Reset |

| 7 | Yes | Set | - |

| 91 | Yes | Reset | - |

+-------+--------------+-------------+--------------+

2. Memory

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| Site Type | Used | Fixed | Available | Util% |

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| Block RAM Tile | 0.5 | 0 | 50 | 1.00 |

| RAMB36/FIFO\* | 0 | 0 | 50 | 0.00 |

| RAMB18 | 1 | 0 | 100 | 1.00 |

| RAMB18E1 only | 1 | | | |

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\* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

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| Site Type | Used | Fixed | Available | Util% |

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| DSPs | 0 | 0 | 90 | 0.00 |

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4. IO and GT Specific

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| Site Type | Used | Fixed | Available | Util% |

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| Bonded IOB | 33 | 0 | 106 | 31.13 |

| Bonded IPADs | 0 | 0 | 10 | 0.00 |

| Bonded OPADs | 0 | 0 | 4 | 0.00 |

| PHY\_CONTROL | 0 | 0 | 5 | 0.00 |

| PHASER\_REF | 0 | 0 | 5 | 0.00 |

| OUT\_FIFO | 0 | 0 | 20 | 0.00 |

| IN\_FIFO | 0 | 0 | 20 | 0.00 |

| IDELAYCTRL | 0 | 0 | 5 | 0.00 |

| IBUFGDS | 0 | 0 | 104 | 0.00 |

| PHASER\_OUT/PHASER\_OUT\_PHY | 0 | 0 | 20 | 0.00 |

| PHASER\_IN/PHASER\_IN\_PHY | 0 | 0 | 20 | 0.00 |

| IDELAYE2/IDELAYE2\_FINEDELAY | 0 | 0 | 250 | 0.00 |

| IBUFDS\_GTE2 | 0 | 0 | 2 | 0.00 |

| ILOGIC | 0 | 0 | 106 | 0.00 |

| OLOGIC | 0 | 0 | 106 | 0.00 |

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5. Clocking

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| Site Type | Used | Fixed | Available | Util% |

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| BUFGCTRL | 1 | 0 | 32 | 3.12 |

| BUFIO | 0 | 0 | 20 | 0.00 |

| MMCME2\_ADV | 0 | 0 | 5 | 0.00 |

| PLLE2\_ADV | 0 | 0 | 5 | 0.00 |

| BUFMRCE | 0 | 0 | 10 | 0.00 |

| BUFHCE | 0 | 0 | 72 | 0.00 |

| BUFR | 0 | 0 | 20 | 0.00 |

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6. Specific Feature

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| Site Type | Used | Fixed | Available | Util% |

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| BSCANE2 | 0 | 0 | 4 | 0.00 |

| CAPTUREE2 | 0 | 0 | 1 | 0.00 |

| DNA\_PORT | 0 | 0 | 1 | 0.00 |

| EFUSE\_USR | 0 | 0 | 1 | 0.00 |

| FRAME\_ECCE2 | 0 | 0 | 1 | 0.00 |

| ICAPE2 | 0 | 0 | 2 | 0.00 |

| PCIE\_2\_1 | 0 | 0 | 1 | 0.00 |

| STARTUPE2 | 0 | 0 | 1 | 0.00 |

| XADC | 0 | 0 | 1 | 0.00 |

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7. Primitives

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| Ref Name | Used | Functional Category |

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| FDRE | 91 | Flop & Latch |

| LUT6 | 64 | LUT |

| LUT1 | 49 | LUT |

| LUT5 | 30 | LUT |

| OBUF | 20 | IO |

| CARRY4 | 16 | CarryLogic |

| IBUF | 13 | IO |

| LUT4 | 11 | LUT |

| LUT3 | 11 | LUT |

| LUT2 | 11 | LUT |

| FDSE | 7 | Flop & Latch |

| RAMB18E1 | 1 | Block Memory |

| BUFG | 1 | Clock |

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8. Black Boxes

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| Ref Name | Used |

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9. Instantiated Netlists

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| Ref Name | Used |

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